CLAIMS

What is claimed is:

1. A method for predicting a clock skew for an incomplete integrated circuit design including at least one clock design figure for routing a clock signal, said method comprising:

selecting, from the top, a first metal layer including at least one clock design figure;

placing, if a minimum clocks skew is to be predicted, clock source locations on the clock design figure in accordance with a first predetermined minimum distance between adjacent clock source locations;

placing, if a maximum clock skew is to be predicted, a clock source location on a first clock design figure having a largest size in the first layer, such that the clock source location has a largest distance from a via to a lower layer; and

placing, if an intermediate clock skew is to be predicted, clock source locations on intersections between the clock design figure and a virtual clock grid created for the first metal layer, the virtual clock grid having a predetermined offset from a design boundary and a predetermined pitch between grid lines.

2. The method in accordance with claim 1, further comprising:

sorting the metal layers from the top; and

identifying, for each metal layer, a direction of the clock design figures in the metal layer.

3. The method in accordance with claim 1, further comprising:

sorting clock design figures in accordance with sizes thereof in each metal layer.

4. The method in accordance with claim 1, further comprising, if the minimum clock skew is to be predicted:

selecting a second metal layer including at least one clock design figure; and

placing clock source locations on the clock design figure in the second metal layer in accordance with a second predetermined minimum distance between adjacent clock source locations, if the clock design figure in the second metal layer is not connected to a clock design figure in an upper metal layer.

5. The method in accordance with claim 4, wherein all of the clock figures in the first metal layer are provided with at least one clock source location.

6. The method in accordance with claim 4, further comprising:

iteratively repeating said selecting a second metal layer and said placing clock source locations in the second metal layer until all of the metal layers including at least one clock design figure are processed.

7. The method in accordance with claim 4, wherein said placing clock source locations includes:

maximizing a number of the clock source locations placed in a clock figure.

8. The method in accordance with claim 1, further comprising, if the maximum clock skew is to be predicted:

selecting a second clock design figure having a next largest size in the first metal layer; and

placing a clock source location on the second clock design figure such that the clock source location has a largest distance from a via to a lower layer, if the second clock design figure is not connected to an already processed clock design figure.

9. The method in accordance with claim 8, further comprising:

iteratively repeating said selecting a second clock design figure and said placing a clock source location on the second clock design figure until all of the clock design figures in the first metal layer are processed.

10. A method in accordance with claim 8, further comprising, if the maximum clock skew is to be predicted:

selecting a second metal layer including at least one clock design figure;

selecting a third clock design figure having a largest size in the second metal layer;

placing a clock source location on the third clock design figure such that the clock source location has a largest distance from a via to a lower layer, if the third clock design figure is not connected to an already processed clock design figure;

selecting a fourth clock design figure having a next largest size in the second metal layer; and

placing a clock source location on the fourth clock design figure such that the clock source location has a largest distance from a via to a lower layer, if the fourth clock design figure is not connected to an already processed clock design figure.

11. A method in accordance with claim 10, further comprising:

iteratively repeating said selecting a fourth clock design figure, and said placing a clock source location on the fourth clock design figure until all of the clock design figures in the second metal layer are processed.

12. The method in accordance with claim 1, further comprising, if the intermediate clock skew is to be predicted:

selecting a second metal layer including at least one clock design figure;

creating a second virtual clock grid for the second metal layer, the second virtual clock grid having a second predetermined offset from a design boundary and a second predetermined pitch; and

placing clock source locations on intersections between the clock design figure in the second metal layer and the second virtual clock grid, if the clock design figure in the second metal layer does not have a connection to a clock design figure in an upper metal layer.

13. The method in accordance with claim 12, wherein all of the clock figures in the first metal layer are provided with at least one clock source location.

14. The method in accordance with claim 12, further comprising:

iteratively repeating said selecting a second metal layer, said creating a second virtual clock grid, and said placing clock source locations in the second metal layer until all of the clock design figures have at least one clock source location provided therein or a connection to a clock design figure in an upper metal layer.

15. The method in accordance with claim 12, further comprising:

changing the offset of a virtual clock grid such that the virtual clock grid intersects a maximum number of clock design figures in a corresponding metal layer.

16. The method in accordance with claim 1, further comprising:

calculating a clock skew of the incomplete circuit design using the placed clock source locations.

17. A method for predicting a clock skew for an incomplete integrated circuit design including at least one clock design figure for routing a clock signal, said method comprising:

selecting, from the top, a first metal layer including at least one clock design figure;

placing clock source locations on the clock design figure in accordance with a first predetermined minimum distance between adjacent clock source locations;

selecting a second metal layer including at least one clock design figure;

determining if the clock design figure in the second metal layer is connected to a clock design figure in an upper metal layer;

placing clock source locations on the clock design figure in the second metal layer in accordance with a second predetermined minimum distance between adjacent clock source locations, if the clock design figure in the second metal layer is not connected to a clock design figure in an upper metal layer; and.

iteratively repeating said selecting a second metal layer, said determining, and said placing clock source locations in the second metal layer until all of the metal layers including at least one clock design figure are processed.

18. A method for predicting a clock skew for an incomplete integrated circuit design including at least one clock design figure for routing a clock signal, said method comprising:

selecting, from the top, a first metal layer including at least one clock design figure;

selecting a first clock design figure having a largest size in the first metal layer;

placing a clock source location on the first clock design figure such that the clock source location has a largest distance from a via to a lower layer;

selecting a second clock design figure having a next largest size in the first metal layer;

determining if the second clock design figure is connected to an already processed clock design figure;

placing a clock source location on the second clock design figure such that the clock source location has a largest distance from a via to a lower layer, if the second clock design figure is not connected to an already processed clock design figure; and

iteratively repeating said selecting a second clock design figure, said determining, and said placing a clock source location on the second clock design figure until all of the clock design figures in the first metal layer are processed.

19. A method in accordance with claim 18, further comprising:

selecting a second metal layer including at least one clock design figure;

selecting a third clock design figure having a largest size in the second metal layer;

determining if the third clock design figure is connected to an already processed clock design figure;

placing a clock source location on the third clock design figure such that the clock source location has a largest distance from a via to a lower layer, if the third clock design figure is not connected to an already processed clock design figure;

selecting a fourth clock design figure having a next largest size in the second metal layer;

determining if the fourth clock design figure is connected to an already processed clock design figure;

placing a clock source location on the fourth clock design figure such that the clock source location has a largest distance from a via to a lower layer, if the fourth clock design figure is not connected to an already processed clock design figure; and

iteratively repeating said selecting a fourth clock design figure, said determining, and said placing a clock source location on the fourth clock design figure until all of the clock design figures in the second metal layer are processed.

20. A method for predicting a clock skew for an incomplete integrated circuit design including at least one clock design figure for routing a clock signal, said method comprising:

selecting, from the top, a first metal layer including at least one clock design figure;

creating a virtual clock grid for the first metal layer, the virtual clock grid having a predetermined offset from a design boundary and a predetermined pitch between grid lines;

placing clock source locations on intersections between the clock design figure and the virtual clock grid;

selecting a second metal layer including at least one clock design figure;

creating a second virtual clock grid for the second metal layer, the second virtual clock grid having a second predetermined offset from a design boundary and a second predetermined pitch;

determining if the clock design figure in the second metal layer is connected to a clock design figure in an upper metal layer;

placing clock source locations on intersections between the clock design figure in the second metal layer and the second virtual clock grid, if the clock design figure in the

second metal layer does not have a connection to a clock design figure in an upper metal layer; and

iteratively repeating said selecting a second metal layer, said creating a second virtual clock grid, said determining, and said placing clock source locations in the second metal layer until all of the clock design figures have at least one clock source location provided therein or a connection to a clock design figure in an upper metal layer.

21. A clock skew prediction tool for an incomplete integrated circuit design including at least one clock design figure for routing a clock signal, said tool comprising:

a layer selector coupled to a database containing the incomplete integrated circuit design, said layer selector being adapted to select, from the top, a metal layer including at least one clock design figure; and

a clock source placer coupled to said layer selector, said clock source placer being adapted to place clock source locations on the clock design figure in a selected metal layer based on a clock skew to be predicted, said clock source placer including at least one of:

a first module for a minimum skew prediction, said first module being adapted to place clock source locations on the clock design figure in accordance with a first predetermined minimum distance between adjacent clock source locations;

a second module for a maximum skew prediction, said second module being adapted to place a clock source location on a first clock design figure having a largest size in the selected layer such that the clock source location has a largest distance from a via to a lower layer; and

a third module for an intermediate skew prediction, said third module being adapted to place clock source locations on intersections between the clock design figure in the selected metal layer and a virtual clock grid created for the selected metal layer, the virtual clock grid having a predetermined offset from a design boundary and a predetermined pitch between grid lines.

22. The tool in accordance with claim 21, wherein said layer selector is adapted to sort the metal layers in accordance with the order from the top of a multi-layered structure in the integrated circuit design.

23. The tool in accordance with claim 21, wherein said clock source placer further includes:

a direction identifier coupled to the database, said direction identifier being adapted to identify a direction of the clock design figures in the selected metal layer.

24. The tool in accordance with claim 21, wherein said clock source placer further includes:

a clock design figure selector coupled to the database, said design figure selector being adapted to sort the clock design figures in accordance with sizes thereof in the selected metal layer.

25. The tool in accordance with claim 21, wherein said clock source placer further includes:

a first connection determiner coupled to said first module and said third module, said first connection determiner being adapted to determine if a clock design figure in the selected metal layer is connected to a clock design figure in an upper metal layer.

26. The tool in accordance with claim 25, wherein said first module is adapted to place at least one clock location on all clock design figures in a first selected metal layer.

27. The tool in accordance with claim 25, wherein said first module is adapted to place at least one clock source location on the clock design figure in a second selected metal layer in accordance with a second predetermined minimum distance between adjacent clock source locations, if the clock design figure in the second selected metal layer is not connected to a clock design figure in an upper metal layer.

28. The tool in accordance with claim 21, wherein said first module is adapted to place the clock source locations so as to maximize a number of the clock source locations placed in a clock design figure.

29. The tool in accordance with claim 21, wherein said clock source placer further includes:

a second connection determiner coupled to said second module, said second connection determiner being adapted to determine if a clock design figure in the selected metal layer is connected to an already processed clock design figure.

30. The tool in accordance with claim 29, wherein said second module further adapted to place a clock source location on a second clock design figure having a next largest size in the selected metal layer, such that the clock source location has a largest distance from a via to a lower layer, if the second clock design figure is not connected to an already processed clock design figure.

31. The tool in accordance with claim 21, wherein said clock source placer further comprising:

a virtual clock grid generator coupled to said third module, said virtual clock grid generator being adapted to create a virtual clock grid for a selected metal layer, the virtual clock grid having a predetermined offset from a design boundary and a predetermined pitch.

32. The tool in accordance with claim 31, wherein said third module is adapted to place at least one clock source location on all clock design figures in a first selected metal layer.

33. The tool in accordance with claim 31, wherein said third module is adapted to place clock source locations on intersections between a clock design figure in a second selected metal layer and a second virtual clock grid, if the clock design figure in the second selected metal layer does not have a connection to a clock design figure in an upper metal layer.

34. The tool in accordance with claim 31, wherein said virtual clock grid generator is adapted to change the offset of a virtual clock grid such that the virtual clock grid intersects a maximum number of clock design figures in a selected metal layer.

35. An apparatus for predicting a clock skew for an incomplete integrated circuit design including at least one clock design figure for routing a clock signal, said apparatus comprising:

means for selecting, from the top, a first metal layer including at least one clock design figure;

means for placing, if a minimum clocks skew is to be predicted, clock source locations on the clock design figure in accordance with a first predetermined minimum distance between adjacent clock source locations;

means for placing, if a maximum clock skew is to be predicted, a clock source location on a first clock design figure having a largest size in the first layer, such that the clock source location has a largest distance from a via to a lower layer; and

means for placing, if an intermediate clock skew is to be predicted, clock source locations on intersections between the clock design figure and a virtual clock grid created for the first metal layer, the virtual clock grid having a predetermined offset from a design boundary and a predetermined pitch between grid lines.

36. The apparatus in accordance with claim 35, further comprising:

means for sorting the metal layers from the top; and

means for identifying, for each metal layer, a direction of the clock design figures in the metal layer.

37. The apparatus in accordance with claim 35, further comprising:

means for sorting clock design figures in accordance with sizes thereof in each metal layer.

38. The apparatus in accordance with claim 35, further comprising, if the minimum clock skew is to be predicted:

means for selecting a second metal layer including at least one clock design figure; and

means for placing clock source locations on the clock design figure in the second metal layer in accordance with a second predetermined minimum distance between adjacent clock source locations, if the clock design figure in the second metal layer is not connected to a clock design figure in an upper metal layer.

39. The apparatus in accordance with claim 38, wherein all of the clock figures in the first metal layer are provided with at least one clock source location.

40. The apparatus in accordance with claim 38, further comprising:

means for iteratively executing said means for selecting a second metal layer and said means for placing clock source locations in the second metal layer until all of the metal layers including at least one clock design figure are processed.

41. The apparatus in accordance with claim 38, wherein means for said placing clock source locations includes:

means for maximizing a number of the clock source locations placed in a clock figure.

42. The apparatus in accordance with claim 35, further comprising, if the maximum clock skew is to be predicted:

means for selecting a second clock design figure having a next largest size in the first metal layer; and

means for placing a clock source location on the second clock design figure such that the clock source location has a largest distance from a via to a lower layer, if the second clock design figure is not connected to an already processed clock design figure.

43. The apparatus in accordance with claim 42, further comprising:

means for iteratively executing said means for selecting a second clock design figure and said means for placing a clock source location on the second clock design figure until all of the clock design figures in the first metal layer are processed.

44. A apparatus in accordance with claim 42, further comprising, if the maximum clock skew is to be predicted:

means for selecting a second metal layer including at least one clock design figure;

means for selecting a third clock design figure having a largest size in the second metal layer;

means for placing a clock source location on the third clock design figure such that the clock source location has a largest distance from a via to a lower layer, if the third clock design figure is not connected to an already processed clock design figure;

means for selecting a fourth clock design figure having a next largest size in the second metal layer; and

means for placing a clock source location on the fourth clock design figure such that the clock source location has a largest distance from a via to a lower layer, if the fourth clock design figure is not connected to an already processed clock design figure.

45. A apparatus in accordance with claim 44, further comprising:

means for iteratively executing said means for selecting a fourth clock design figure, and said means for placing a clock source location on the fourth clock design figure until all of the clock design figures in the second metal layer are processed.

46. The apparatus in accordance with claim 35, further comprising, if the intermediate clock skew is to be predicted:

means for selecting a second metal layer including at least one clock design figure;

means for creating a second virtual clock grid for the second metal layer, the second virtual clock grid having a second predetermined offset from a design boundary and a second predetermined pitch; and

means for placing clock source locations on intersections between the clock design figure in the second metal layer and the second virtual clock grid, if the clock design figure in the second metal layer does not have a connection to a clock design figure in an upper metal layer.

47. The apparatus in accordance with claim 46, wherein all of the clock figures in the first metal layer are provided with at least one clock source location.

48. The apparatus in accordance with claim 46, further comprising:

means for iteratively executing said means for selecting a second metal layer, said means for creating a second virtual clock grid, and said means for placing clock source locations in the second metal layer until all of the clock design figures have at least one clock source location provided therein or a connection to a clock design figure in an upper metal layer.

49. The apparatus in accordance with claim 46, further comprising:

means for changing the offset of a virtual clock grid such that the virtual clock grid intersects a maximum number of clock design figures in a corresponding metal layer.

50. The apparatus in accordance with claim 35, further comprising:

means for calculating a clock skew of the incomplete circuit design using the placed clock source locations.

51. A apparatus for predicting a clock skew for an incomplete integrated circuit design including at least one clock design figure for routing a clock signal, said apparatus comprising:

means for selecting, from the top, a first metal layer including at least one clock design figure;

means for placing clock source locations on the clock design figure in accordance with a first predetermined minimum distance between adjacent clock source locations;

means for selecting a second metal layer including at least one clock design figure;

means for determining if the clock design figure in the second metal layer is connected to a clock design figure in an upper metal layer;

means for placing clock source locations on the clock design figure in the second metal layer in accordance with a second predetermined minimum distance between adjacent clock source locations, if the clock design figure in the second metal layer is not connected to a clock design figure in an upper metal layer; and.

means for iteratively executing said means for selecting a second metal layer, said means for determining, and said means for placing clock source locations in the second metal layer until all of the metal layers including at least one clock design figure are processed.

52. A apparatus for predicting a clock skew for an incomplete integrated circuit design including at least one clock design figure for routing a clock signal, said apparatus comprising:

means for selecting, from the top, a first metal layer including at least one clock design figure;

means for selecting a first clock design figure having a largest size in the first metal layer;

means for placing a clock source location on the first clock design figure such that the clock source location has a largest distance from a via to a lower layer;

means for selecting a second clock design figure having a next largest size in the first metal layer;

means for determining if the second clock design figure is connected to an already processed clock design figure;

means for placing a clock source location on the second clock design figure such that the clock source location has a largest distance from a via to a lower layer, if the second clock design figure is not connected to an already processed clock design figure; and

means for iteratively executing said means for selecting a second clock design figure, said means for determining, and said means for placing a clock source location on the second clock design figure until all of the clock design figures in the first metal layer are processed.

53. A apparatus in accordance with claim 52, further comprising:

means for selecting a second metal layer including at least one clock design figure;

means for selecting a third clock design figure having a largest size in the second metal layer;

means for determining if the third clock design figure is connected to an already processed clock design figure;

means for placing a clock source location on the third clock design figure such that the clock source location has a largest distance from a via to a lower layer, if the third clock design figure is not connected to an already processed clock design figure;

means for selecting a fourth clock design figure having a next largest size in the second metal layer;

means for determining if the fourth clock design figure is connected to an already processed clock design figure;

means for placing a clock source location on the fourth clock design figure such that the clock source location has a largest distance from a via to a lower layer, if the fourth clock design figure is not connected to an already processed clock design figure; and

means for iteratively executing said means for selecting a fourth clock design figure, said means for determining, and said means for placing a clock source location on the fourth clock design figure until all of the clock design figures in the second metal layer are processed.

54. A apparatus for predicting a clock skew for an incomplete integrated circuit design including at least one clock design figure for routing a clock signal, said apparatus comprising:

means for selecting, from the top, a first metal layer including at least one clock design figure;

means for creating a virtual clock grid for the first metal layer, the virtual clock grid having a predetermined offset from a design boundary and a predetermined pitch between grid lines;

means for placing clock source locations on intersections between the clock design figure and the virtual clock grid;

means for selecting a second metal layer including at least one clock design figure;

means for creating a second virtual clock grid for the second metal layer, the second virtual clock grid having a second predetermined offset from a design boundary and a second predetermined pitch;

means for determining if the clock design figure in the second metal layer is connected to a clock design figure in an upper metal layer;

means for placing clock source locations on intersections between the clock design figure in the second metal layer and the second virtual clock grid, if the clock design figure in the second metal layer does not have a connection to a clock design figure in an upper metal layer; and

means for iteratively executing said means for selecting a second metal layer, said means for creating a second virtual clock grid, said means for determining, and means for said placing clock source locations in the second metal layer until all of the clock design figures have at least one clock source location provided therein or a connection to a clock design figure in an upper metal layer.

55. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method for predicting a clock skew for an incomplete integrated circuit design including at least one clock design figure for routing a clock signal, said method comprising:

selecting, from the top, a first metal layer including at least one clock design figure;

placing, if a minimum clocks skew is to be predicted, clock source locations on the clock design figure in accordance with a first predetermined minimum distance between adjacent clock source locations;

placing, if a maximum clock skew is to be predicted, a clock source location on a first clock design figure having a largest size in the first layer, such that the clock source location has a largest distance from a via to a lower layer; and

placing, if an intermediate clock skew is to be predicted, clock source locations on intersections between the clock design figure and a virtual clock grid created for the first metal layer, the virtual clock grid having a predetermined offset from a design boundary and a predetermined pitch between grid lines.

56. The program storage device in accordance with claim 55, wherein said method further comprises, if the minimum clock skew is to be predicted:

selecting a second metal layer including at least one clock design figure; and

placing clock source locations on the clock design figure in the second metal layer in accordance with a second predetermined minimum distance between adjacent clock

source locations, if the clock design figure in the second metal layer is not connected to a clock design figure in an upper metal layer.

57. The program storage device in accordance with claim 56, wherein said method further comprises:

iteratively repeating said selecting a second metal layer and said placing clock source locations in the second metal layer until all of the metal layers including at least one clock design figure are processed.

58. The program storage device in accordance with claim 55, wherein said method further comprises, if the maximum clock skew is to be predicted:

selecting a second clock design figure having a next largest size in the first metal layer; and

placing a clock source location on the second clock design figure such that the clock source location has a largest distance from a via to a lower layer, if the second clock design figure is not connected to an already processed clock design figure.

59. The program storage device in accordance with claim 58, wherein said method further comprises:

iteratively repeating said selecting a second clock design figure and said placing a clock source location on the second clock design figure until all of the clock design figures in the first metal layer are processed.

60. The program storage device in accordance with claim 58, wherein said method further comprises, if the maximum clock skew is to be predicted:

selecting a second metal layer including at least one clock design figure;

selecting a third clock design figure having a largest size in the second metal layer;

placing a clock source location on the third clock design figure such that the clock source location has a largest distance from a via to a lower layer, if the third clock design figure is not connected to an already processed clock design figure;

selecting a fourth clock design figure having a next largest size in the second metal layer; and

placing a clock source location on the fourth clock design figure such that the clock source location has a largest distance from a via to a lower layer, if the fourth clock design figure is not connected to an already processed clock design figure.

61. The program storage device in accordance with claim 60, wherein said method further comprises:

iteratively repeating said selecting a fourth clock design figure, and said placing a clock source location on the fourth clock design figure until all of the clock design figures in the second metal layer are processed.

62. The program storage device in accordance with claim 55, wherein said method further comprises, if the intermediate clock skew is to be predicted:

selecting a second metal layer including at least one clock design figure;

creating a second virtual clock grid for the second metal layer, the second virtual clock grid having a second predetermined offset from a design boundary and a second predetermined pitch; and

placing clock source locations on intersections between the clock design figure in the second metal layer and the second virtual clock grid, if the clock design figure in the second metal layer does not have a connection to a clock design figure in an upper metal layer.

63. The program storage device in accordance with claim 62, wherein said method further comprises:

iteratively repeating said selecting a second metal layer, said creating a second virtual clock grid, and said placing clock source locations in the second metal layer until all of the clock design figures have at least one clock source location provided therein or a connection to a clock design figure in an upper metal layer.

64. The program storage device in accordance with claim 62, wherein said method further comprises:

changing the offset of a virtual clock grid such that the virtual clock grid intersects a maximum number of clock design figures in a corresponding metal layer.

65. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method for predicting a clock

skew for an incomplete integrated circuit design including at least one clock design figure for routing a clock signal, said method comprising:

selecting, from the top, a first metal layer including at least one clock design figure;

placing clock source locations on the clock design figure in accordance with a first predetermined minimum distance between adjacent clock source locations;

selecting a second metal layer including at least one clock design figure;

determining if the clock design figure in the second metal layer is connected to a clock design figure in an upper metal layer;

placing clock source locations on the clock design figure in the second metal layer in accordance with a second predetermined minimum distance between adjacent clock source locations, if the clock design figure in the second metal layer is not connected to a clock design figure in an upper metal layer; and.

iteratively repeating said selecting a second metal layer, said determining, and said placing clock source locations in the second metal layer until all of the metal layers including at least one clock design figure are processed.

66. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method for predicting a clock skew for an incomplete integrated circuit design including at least one clock design figure for routing a clock signal, said method comprising:

selecting, from the top, a first metal layer including at least one clock design figure;

selecting a first clock design figure having a largest size in the first metal layer;

placing a clock source location on the first clock design figure such that the clock source location has a largest distance from a via to a lower layer;

selecting a second clock design figure having a next largest size in the first metal layer;

determining if the second clock design figure is connected to an already processed clock design figure;

placing a clock source location on the second clock design figure such that the clock source location has a largest distance from a via to a lower layer, if the second clock design figure is not connected to an already processed clock design figure; and

iteratively repeating said selecting a second clock design figure, said determining, and said placing a clock source location on the second clock design figure until all of the clock design figures in the first metal layer are processed.

67. The program storage device in accordance with claim 66, wherein said method further comprises:

selecting a second metal layer including at least one clock design figure;

selecting a third clock design figure having a largest size in the second metal layer;

determining if the third clock design figure is connected to an already processed clock design figure;

placing a clock source location on the third clock design figure such that the clock source location has a largest distance from a via to a lower layer, if the third clock design figure is not connected to an already processed clock design figure;

selecting a fourth clock design figure having a next largest size in the second metal layer;

determining if the fourth clock design figure is connected to an already processed clock design figure;

placing a clock source location on the fourth clock design figure such that the clock source location has a largest distance from a via to a lower layer, if the fourth clock design figure is not connected to an already processed clock design figure; and

iteratively repeating said selecting a fourth clock design figure, said determining, and said placing a clock source location on the fourth clock design figure until all of the clock design figures in the second metal layer are processed.

68. A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method for predicting a clock skew for an incomplete integrated circuit design including at least one clock design figure for routing a clock signal, said method comprising:

selecting, from the top, a first metal layer including at least one clock design figure;

creating a virtual clock grid for the first metal layer, the virtual clock grid having a predetermined offset from a design boundary and a predetermined pitch between grid lines;

placing clock source locations on intersections between the clock design figure and the virtual clock grid;

selecting a second metal layer including at least one clock design figure;

creating a second virtual clock grid for the second metal layer, the second virtual clock grid having a second predetermined offset from a design boundary and a second predetermined pitch;

determining if the clock design figure in the second metal layer is connected to a clock design figure in an upper metal layer;

placing clock source locations on intersections between the clock design figure in the second metal layer and the second virtual clock grid, if the clock design figure in the second metal layer does not have a connection to a clock design figure in an upper metal layer; and

iteratively repeating said selecting a second metal layer, said creating a second virtual clock grid, said determining, and said placing clock source locations in the second metal layer until all of the clock design figures have at least one clock source location provided therein or a connection to a clock design figure in an upper metal layer.